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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	)
Michael A. Marra et al.	) Group: 2121
Serial No.: 09/226,971	)
Filed: January 8, 1999	)
Title: METHOD OF REGULATING A TARGET	)
SYSTEM USING A FREQUENCY	)
COMPARISON OF FEEDBACK AND	)
REFERENCE PULSE TRAINS	) Examiner: S. R. Garland

REPLY BRIEF OF APPELLANT

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Washington, D.C. 20231

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Sir:

Responsive to the Examiner's Answer dated April 8, 2002, Appellants submit the following Reply Brief.

Responsive to the Examiner's argument that claims 1 and 8 of Appellants' invention are anticipated by U.S. Patent No. 5,212,434 (Hsieh) under 35 U.S.C. § 102(b), Appellants submit that:

Hsieh does not teach, disclose or suggest the comparison of frequencies and the generation of a control signal based on that comparison, as recited in part by claim 1.

Claim 1 recites in part:

> generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;
>
> providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a

frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train; and

generating a control signal based upon said comparison.

(Emphasis added) Appellants submit that such an invention is not taught, disclosed nor suggested by the cited references, alone or in combination, and includes distinct advantages thereover.

The Examiner contends that element 10 serves to compare the reference pulse train frequency to the feedback pulse train frequency. However, phase detector 10 serves to compare the phases of two input signals.

The Hsieh disclosure, starting at column 4, line 12, recites in part:

> The phase detector 10 is capable of comparing ... the difference between the phase θ_1 of the feedback signal $P_1(t)$ and the phase θ_2 of the reference signal $P_2(t)$ and generating thereby a square pulse ... in proportion to the phase error θ_e.

(Emphasis Added). Appellants' invention is not concerned with the phase of two signals, rather Appellants' invention, as recited in claim 1, compares the frequency of two signals. Herein lies a major advantage of Appellants' invention, in that the complexity of phase comparison of two signals is obviated and the cost thereof is eliminated. Hsieh measures phase differences of two signals and controls the speed of a target system to minimize the phase differences thereof. In contrast, Appellants' invention, as recited in claim 1, has features not disclosed in the cited references, in that Appellants' invention generates a reference pulse train, compares the frequency of the reference pulse train with the frequency of a feedback pulse train and generates a control signal based upon the comparison, which is not disclosed, taught or suggested in Hsieh by itself or in combination with any other cited reference.

The Examiner argues that Hsieh compares the frequency of a reference pulse train with the frequency of a feedback pulse train. As stated above, Appellants see no such disclosure in Hsieh. Lacking any disclosure of such a comparison of frequencies, the Examiner states that to, "perform phase comparison inherently requires first that the frequencies of the signals being compared be equal so that the phase difference between the two signals can be determined. Otherwise the phase comparison can not be performed." (Emphasis Added) *Examiner's Answer, page 4.*

Hsieh makes no mention of any reliance on a frequency comparison to determine if the frequencies are equal, as a precursor to performing a phase comparison. Rather Hsieh ensures that the speed of step motor 50 corresponds to the frequency of a reference signal by minimizing the phase difference between the reference signal and a feedback signal from speed detector 60. While it may be assumed that the frequencies of the feedback signal and the reference signal are the same, this is not the result of a frequency comparison, it is rather the result of the minimization of a phase difference between two waveforms.

A phase-locked loop is defined as, "An electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal." *Federal Standard 1037C, Glossary of Telecommunication Terms, August 7, 1996.* This definition is contra to the Examiner's assertion, in that it does not require that the oscillator be operating at the same frequency as the reference signal, rather that only a constant phase angle be maintained. In fact many phase-locked circuits specifically exclude the possibility that the reference signal, and the signal to which it is compared, are the same frequency.

For example see, U.S. Patent 5,608,354 (Hori) entitled, "Phase-Locked Loop Circuit Obtaining The Phase Difference Between Time Series Pulse Strings and a Reference Frequency." In Hori, a phase comparison section detects the phase differences between pulse strings and a reference frequency signal. Abstract, Hori. Figs. 2-5 of Hori illustrate that the pulse strings have fewer pulses than the reference signal. Therefore the Examiner's statement that phase comparison cannot be performed unless the frequencies of the reference pulse train and the feedback pulse train are the same is unfounded.

Assuming arguendo that Hsieh does compare the reference pulse train frequency to the feedback pulse train frequency (which assumption Appellants strongly denies), it is the Appellants' position that Hsieh does not generate a control signal based on a comparison of the frequencies, as recited in part by claim 1. Rather, Hsieh has a phase detector 10 having a first input port V, a second input port R, an output $V_1(t)$ and a phase error output θ_e. First input port V is connected to the output of speed detector 60 to receive feedback signal $P_1(t)$ having phase θ_1 and second input port R is connected to reference signal $P_2(t)$ whose phase is θ_2. The difference between the phase θ_1 of feedback signal $P_1(t)$ and phase θ_2 of reference signal $P_2(t)$ is the phase error θ_e ($\theta_e = \theta_1 - \theta_2$) (Fig.1 and column 3, line 47, through column 4, line 18). It is phase error θ_e which causes up-down counter 22 to increase or decrease proportional to $\theta_e / 2\pi$, the count of which is utilized to alter output voltage V_o, which is proportional to θ_e as shown in Fig. 5 (column 5, lines 27-44). V_o increases if θ_e indicates a phase lag, causing an increase in the rate of pulses sent to motor 50 in order to increase the speed of motor 50. Conversely, V_o decreases if θ_e indicates a phase lead, causing a decrease in the rate of pulses sent to motor 50 in order to decrease the speed of motor 50 (column 5, lines 46-63). Therefore the control signal generated

by Hsieh, is the result of a comparison of phase θ_1 of feedback signal $P_1(t)$ and phase θ_2 of reference signal $P_2(t)$, rather than a control signal generated by a comparison of frequencies, as is claimed in part by claim 1.

In summary, Hsieh does not teach, disclose or suggest generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal, comparing the frequency of the reference pulse train with the frequency of the feedback pulse train, and generating a control signal based upon the comparison as recited, in part, in claim 1.

The present invention, as recited in claim 1, includes distinct advantages over Hsieh. One advantage of the Appellants' invention is that fewer circuit elements and less space is needed for the frequency comparison circuitry than the phase detection circuitry of the references, since comparison of the relative phases of two signals and the generation of a phase error correction signal are not necessary, as they are in the cited references. Another advantage of the Appellants' invention is that phase differences are not detected and not corrected; as a result thereof the circuitry of Appellants' invention has a reduced cost of implementation. Whereas, Appellants' invention is more economically implemented than a phase error detection method, the use of Appellants' invention will find broad appeal in design scenarios, where the detection of phases of signals is cost prohibitive.

The Examiner has stated that the choice of using a microprocessor or discrete circuitry impacts the space requirement and cost, to which Appellants agree. However, the Appellants' invention uses less space at less cost than Hsieh, when the choice of the implementing circuit technology is the same for each.

For all of the foregoing reasons, Appellants submit that claim 1, and claim 8 depending

therefrom, are in condition for allowance, the allowance of which is hereby respectfully requested.

Responsive to the Examiner's argument that Claims 2, 3 and 5 of Appellants' invention are unpatentable over U.S. Patent No. 5,212,434 (Hsieh) in view of either U.S. Patent No. 4,494,509 (Long) or U.S. Patent No. 6,043,695 (O'Sullivan) under 35 U.S.C. § 103(a), Appellants submit that:

The references, taken alone or in combination, fail to teach, disclose or suggest, alone or in combination, the comparison of frequencies, the generation of a control signal based on that comparison and substantially aligning a leading edge of each digital signal in the reference pulse signal with a leading edge of the feedback signal, as recited in part by claim 2.

Claim 2 (incorporating the limitations of base claim 1) recites in part:

> generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;
>
> providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;
>
> comparing said frequency of said reference pulse train with said frequency of said feedback pulse train ... wherein said comparing step comprises substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train; and
>
> generating a control signal based upon said comparison.

(Emphasis added) Appellants submit that such an invention is not taught, disclosed nor suggested

by the cited references, alone or in combination, and includes distinct advantages thereover.

Claims 2, 3 and 5 depend from claim 1, which is in condition for allowance for the reasons given above. Therefore the foregoing arguments also pertain to claims 2, 3 and 5. Accordingly, claims 2, 3 and 5 are in condition for allowance because of their dependency from claim 1. Moreover claims 3 and 5 depend from claim 2, which, with the incorporation of the limitations of claim 1, is separately patentable.

The Examiner states that Hsieh does not disclose that the leading edges of pulses are used by a phase comparator to determine an error but that Long and O'Sullivan teach the comparing of leading edges of pulse trains for determining a phase error. *Examiner's Answer, page 6.* Appellants agree that each of the three cited references teach the determination of a phase error between signals and that Long and O'Sullivan specifically teach the use of the leading edges of two signals to determine a phase error. However, Appellants invention does not compare leading edges of pulse trains, nor does it determine a phase error. In contrast to the cited references, Appellants invention, as recited in claim 2, substantially aligns the leading edge of a reference pulse with a leading edge of a feedback pulse as a part of the comparing step and no comparison or measurement of the differences in leading edge timing is undertaken. Whereas, Appellants' invention intentionally substantially aligns the leading edges of the reference pulses with the leading edges of the feedback pulses as a part of a comparing step, if such a limitation were a part of Hsieh, Long and/or O'Sullivan it would render their phase error detection non-functional. In the cited references, if the reference pulses are aligned with the feedback pulses during a comparison step of the pulses, the sought after detection of phase error, between the leading edges of the two signals, would be null resulting in no change in the control signal, even though

the phases of the signals shift before the signals are aligned. None of the cited references, alone or in combination, teaches, discloses or suggests generating a plurality of digital signals, defining a reference pulse train with a frequency dependent upon said reference signal, ... comparing the frequency of the reference pulse train with the frequency of the feedback pulse train by substantially aligning a leading edge of each digital signal in the reference pulse train with a leading edge of each digital signal in the feedback pulse train, as recited, in part, in claim 2.

Appellants' invention, as recited in claim 2, includes distinct advantages over the cited references. One advantage of the Appellants' invention is that less space is needed for the frequency comparison circuitry than the phase detection circuitry of the references, since comparison of the relative phases of two signals and the generation of a phase error correction signal are not necessary, as they are in the cited references. Another advantage of the Appellants' invention is that phase differences are not detected and not corrected; as a result thereof the circuitry of Appellants' invention has a reduced cost of implementation. Whereas, Appellants' invention is more economically implemented than a phase error detection method, the use of Appellants' invention will find broad appeal in design scenarios, where the controlling of a target by detecting phases of signals is cost prohibitive.

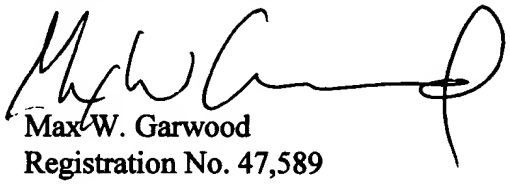
The Examiner has stated that the choice of using a microprocessor or discrete circuitry impacts the space requirement and cost, to which Appellants agree. However, the Appellants' invention uses less space at less cost than the cited references, when the choice of the implementing circuit technology is the same for each.

For all of the foregoing reasons, Appellants submit that claim 2, and claims 3 and 5 depending therefrom, are in condition for allowance, the allowance of which is hereby

respectfully requested.

For the foregoing reasons, Appellant submits that claims 1-3, 5 and 8 are neither anticipated nor suggested by the cited references, alone or in combination, and are therefore in condition for allowance in their present form. Accordingly, Appellants respectfully request the Board to reverse the final rejections of the appealed claims.

Respectfully submitted,



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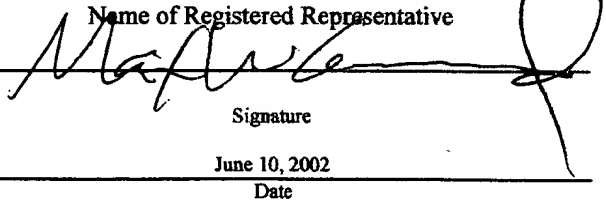

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